MDC Recommendations for Azalia Implementation

December 2003

Document Number: 254122-002

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Revision History

Document Number	Revision Number	Description	Revision Date
254122	001	Initial release	October 2003
254122	002	Updates include: • Updated Section 2.3 • Updated Chapter 3 — Grouped sections for clarity: MDC1.0 Connector and Interface sections now back to back and MDC1.5 Connector and Interface sections are back to back. • Added Figure 18	December 2003

1 Introduction

The Azalia mobile daughter card (MDC) specification provides a mobile form-factor module and interface for audio/modem codec solutions based upon the Azalia Specification. The MDC specification is open to the industry to facilitate IHV validation on Azalia based codec designs. The objective is to produce a specification that will provide an appropriate mobile form factor module that is interoperable and can be placed in the Mott Canyon2 riser card for validation and production.

This specification defines the MDC architecture, required electrical characteristics of the daughter card interface, and mechanical form factor requirements. The document is based on the Azalia Specification, Revision 0.7.

Intel may make changes to specifications and product descriptions at any time, without notice. The reader should verify that the recommendations in this document are in alignment with the most current Azalia specification. This document is not intended to eliminate any features or form factor options that were documented in the original *Mobile Audio/Modem Daughter Card Specification, Revision 1.0*. Please refer to the original document for reference.

1.1 Related Documents

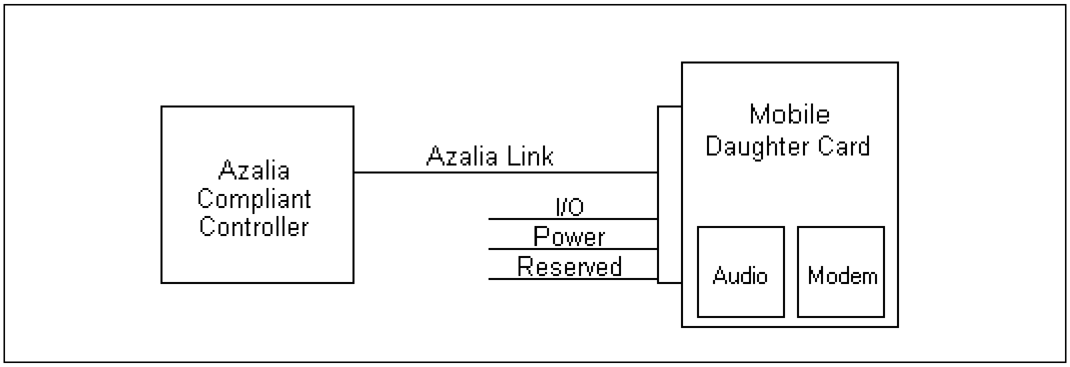
- *Azalia Specification Revision 0.7* – May 5, 2003
- *Mott Canyon II Technical Specification Revision 1.0*
- *Mobile Audio/Modem Daughter Card Specification Revision 1.0*

2 Architectural Overview

2.1 Baseline Architecture

Figure 1 illustrates the baseline architecture of an audio and modem subsystem implementing the mobile daughter card. The MDC can be available in two configurations: a singular functionality option (either modem-only or audio-only module) and a dual functionality option (an audio and modem module).

Figure 1. Baseline Audio/Modem MDC



The system interconnect of the MDC is an Azalia compliant link. Additional signals on the MDC system interface support:

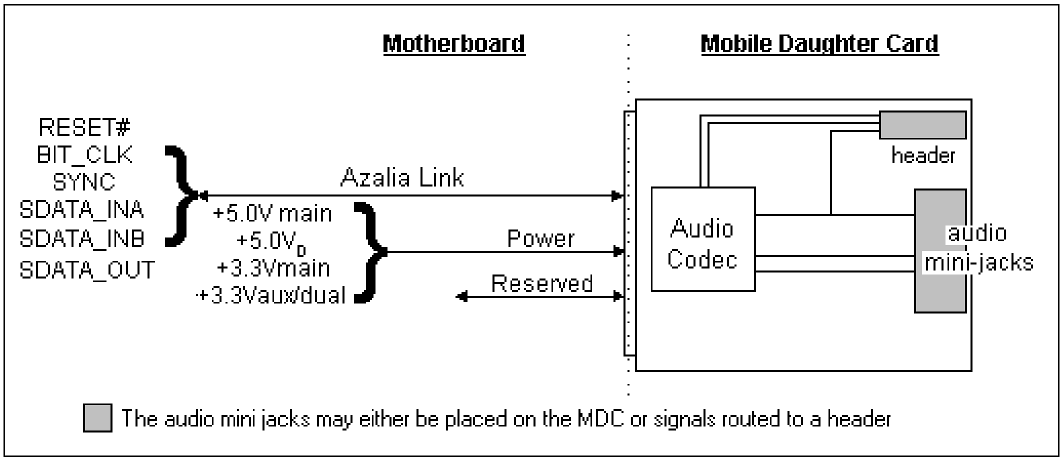
- **I/O:** Includes signals used in split partition codec implementation (e.g., audio codec on the motherboard, modem codec on the daughter card), signals to support audio signals commonly routed on the motherboard (e.g., CD-ROM analog audio signals), and an additional GPIO for amplifier control. These signals also include legacy analog I/O for call progress monitoring.
- **Power:** Signals required to support instantly available PC power management including wake-on-ring (WOR) as well as the main power supplies to operate the audio and modem circuitry on the MDC.
- **Reserved:** Signals reserved for future expansion/modifications of the system interface. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

2.2 Audio/Modem MDC Configurations

2.2.1 Audio–Only MDC

Figure 2 below diagrams an audio-only daughter card implementation with a single Azalia audio codec. Audio-only configurations must include the audio codec and additional amplifiers on the MDC. The audio mini jacks may either be placed on the MDC or signals routed to a header.

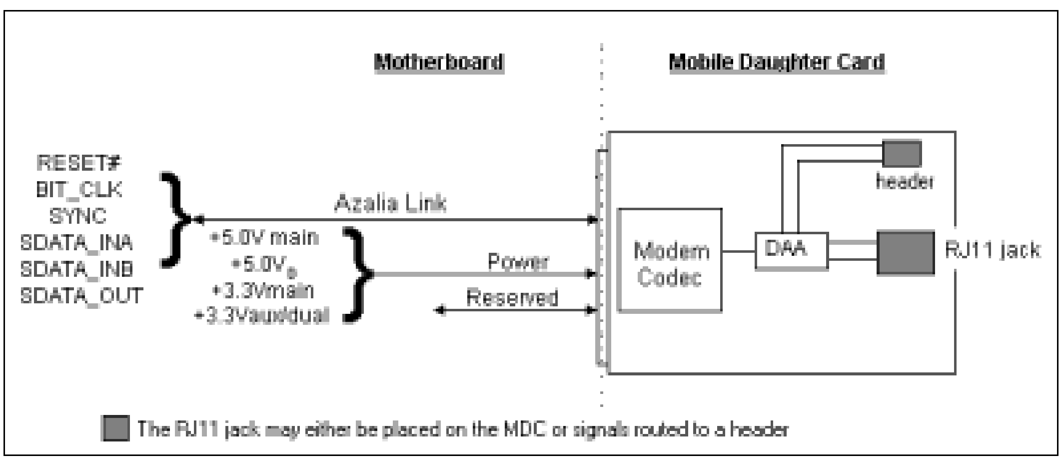
Figure 2. Audio-Only MDC Implementation



2.2.2 Modem–Only MDC

Figure 3 below diagrams a modem-only daughter card implementation with a single Azalia modem codec. Modem-only configurations must include the modem codec and the DAA on the MDC. The RJ11 jack may either be placed on the MDC or signals routed to a header.

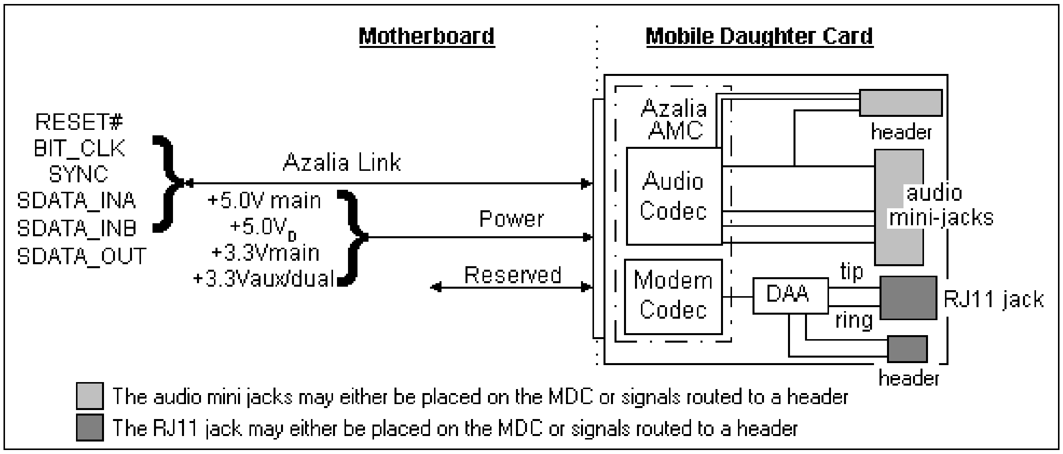
Figure 3. Modem-Only MDC Implementation



2.2.3 Audio and Modem MDC

Figure 4 below diagrams a combined audio and modem MDC module. The audio-and-modem MDC can support either a combined Azalia audio-modem codec or a split Azalia audio codec and Azalia modem codec on the daughter card. Codecs and supporting circuitry must be implemented on the MDC. The RJ11 jack may either be placed on the MDC or signals routed to a header, and the audio mini jacks may either be placed on the MDC or signals routed to a header.

Figure 4. Audio and Modem MDC Implementation



2.3 MDC Audio Requirements

All audio codec implementation requirements in the Azalia Specification apply to the MDC design. Intel recommends that each MDC utilize at least one input jack and one output jack for validation. SPDIF implementation is optional.

The Azalia specification requires codecs providing more than two pluggable jacks to support a single pin to detect the presence of plugs in up to four jacks; up to eight jacks must be detectable with two pins, etc. Each jack must have an isolated switch (normally open) as shown in Figure 5, which closes when a plug is inserted into that jack. The codec measures the impedance of the parallel resistor network to determine which jacks have plugs inserted. Assignment of jacks to sense pins and resistor values are defined in the Azalia Specification and shown in Table 1below.

To ensure physical interoperability between MDCs the parallel resistor network must be powered by the MDC and any supporting circuitry such as resistor pull-ups or filtering capacitors must be implemented on the MDC.

Figure 5. Jack Detect Circuit

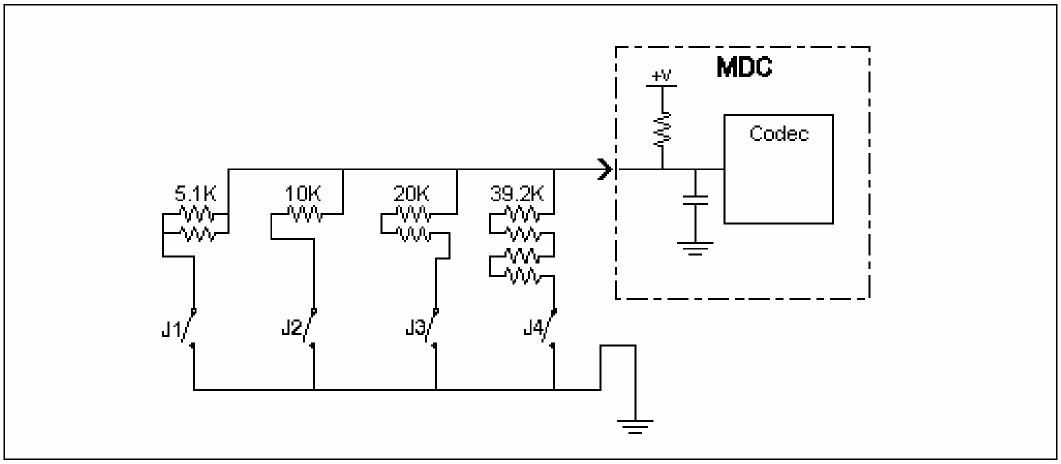


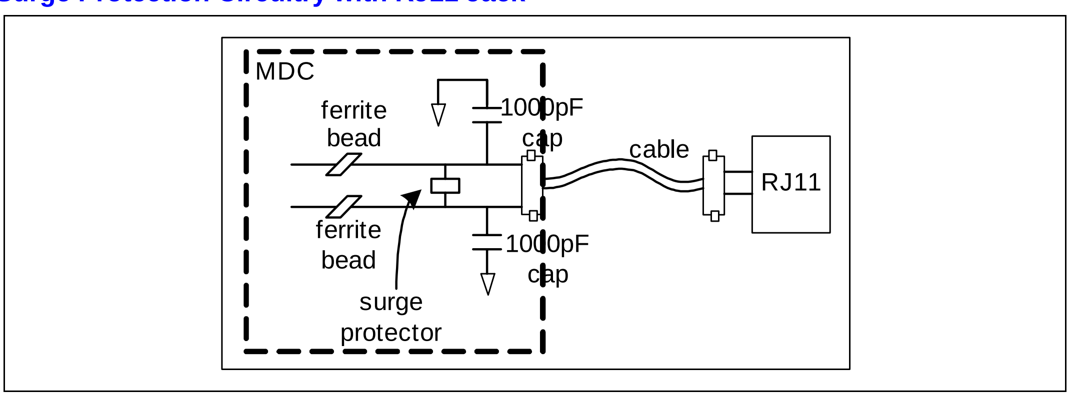
Table 1. Jack Detect Resistor Assignments

Resistors	Sense Pin A	Sense Pin B
39.2 kΩ ± 1%	Jack-A	Jack-E
20 kΩ ± 1%	Jack-B	Jack-F
10 kΩ ± 1%	Jack-C	Jack-G
5.1 kΩ ± 1%	Jack-D	Jack-H

2.4 MDC Modem Requirements

Figure 6 shows a **generic** design of the RJ11 and surge protection circuitry. This isolation circuitry is required on the MDC for the modem codec and DAA.

Figure 6. Surge Protection Circuitry with RJ11 Jack



3 System Interface

3.1 System Interface Connector

3.1.1 MDC 1.0 Connector

The MDC 1.0 system connector is the interface between the motherboard and the audio and/or modem circuitry located on the MDC. The system interface connector is a 30-pin, AMP* 0.8 mm fine pitch SMT connector or equivalent. The connector has low profile, variable parallel board stacking height with a minimum of 3 mm to a maximum of 4.5 mm. The plug (Part Number 3-179396-0) - as shown in Figure 7- is situated on the daughter card. The receptacle (Part Number 3-179397-0) - as shown in Figure 8- is mounted on the motherboard.

Figure 7. 30-Pin AMP* 0.8-mm Fine Pitch SMT Connector Plug

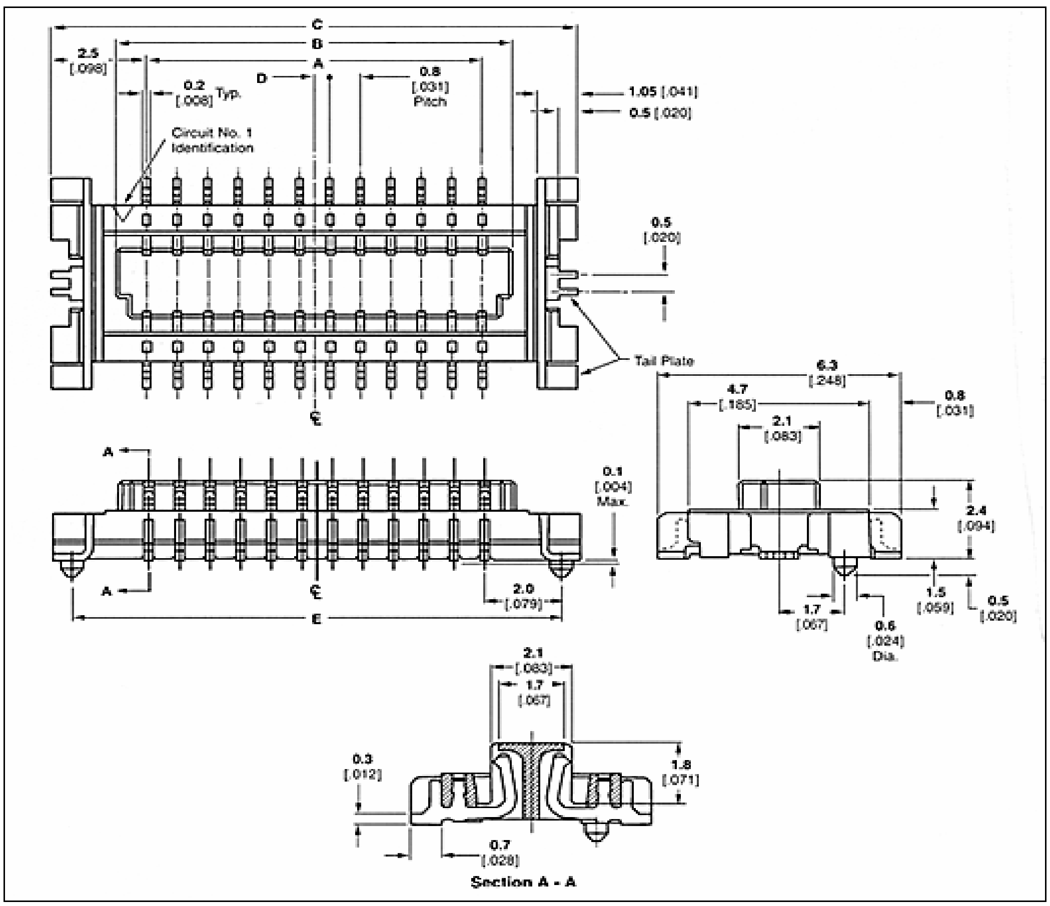


Table 2. Features of 30-Pin AMP* SMT Connector Plug

Features of 30-Pin AMP* Fine Pitch SMT Connector Plug	
Sex	Plug
# of Positions	30
# of Rows	Dual
Centerline Spacing	.031 [0.8] in. [mm]
Keyed	Yes
Board-to-Board Stack Height	.118 [3.00] in. [mm]
Connector Size	.031 [0.8] in. [mm]
Contact Mating Area Plating	Tin-Lead
Locating Posts	With
Packaging Method	Tape Mounted
Dim. A	.441 [11.20] in. [mm]
Dim. B	.502[12.75] in. [mm]
Dim. C	.638[16.2] in. [mm]
Dim. E	.598 [15.20] in. [mm]
Housing Material	6T Nylon
Housing Color	Natural
Housing Material Temp.	High
Contact Material	Phosphor Bronze
Solder Tail Plating	Tin-Lead

Figure 8. 30-Pin AMP* 0.8-mm Fine Pitch SMT Connector Receptacle

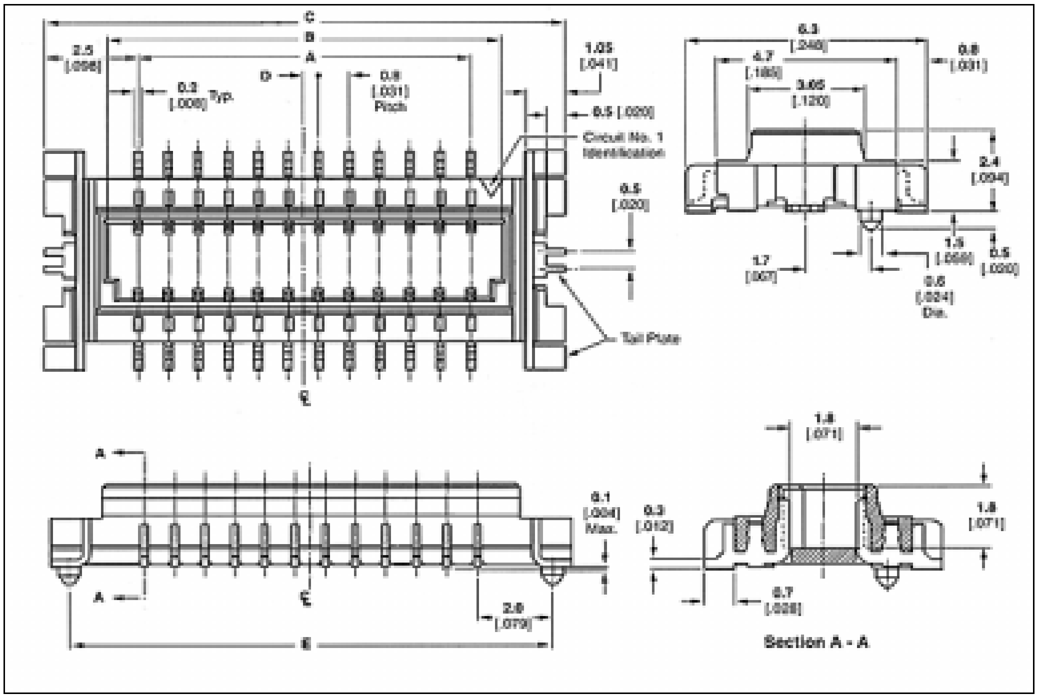


Table 3. Features of 30-Pin AMP* SMT Connector Receptacle

Features of 30-Pin AMP* Fine Pitch SMT Connector Receptacle	
Sex	Receptacle
# of Positions	30
# of Rows	Dual
Centerline Spacing	.031 [0.8] in. [mm]
Keyed	Yes
Board-to-Board Stack Height	.118 [3.00] in. [mm]
Connector Size	.031 [0.8] in. [mm]
Contact Mating Area Plating	Tin-Lead
Locating Posts	With
Packaging Method	Tape Mounted
Dim. A	.441 [11.20] in. [mm]
Dim. B	.504 [12.80] in. [mm]
Dim. C	.638[16.2] in. [mm]
Dim. E	.598 [15.20] in. [mm]
Housing Material	6T Nylon
Housing Color	Natural
Housing Material Temp.	High
Contact Material	Phosphor Bronze
Solder Tail Plating	Tin-Lead

3.1.2 MDC 1.0 Interface

Table 4. Pin-Out for MDC 1.0 Interface

Pin	Signal	Signal	Pin
1	NC	NC	2
3	GND	NC	4
5	NC	RESERVED	6
7	NC	GND	8
9	CD_GND	5 V_{main}	10
11	CD_Right	RESERVED	12
13	CD_Left	RESERVED	14
15	GND	NC	16
17	3.3 $V_{aux/dual}$	5 V_D	18
19	GND	GND	20
21	3.3 V_{main}	Azalia_SYNC	22
23	Azalia_SDO	Azalia_SDI_B	24
25	Azalia_RST#	Azalia_SDI_A	26
27	GND	GND	28
29	NC	Azalia_BCLK	30

3.1.2.1 MDC 1.0 Azalia Pin Descriptions

Table 5. Azalia Pin List for MDC 1.0

Signal Name	Type	Pin Number	Description
Azalia_BCLK	Input	30	Bit Clock: 24.00-MHz clock from the Azalia controller connects to all codecs on the link.
Azalia_SYNC	Input	22	Signal that marks the input and output frame boundaries, as well as identifying outbound data streams. Sourced from the Azalia controller and connects to all codecs on the link.
Azalia_RST#	Input	25	Active low Azalia Link reset signal. Sourced from the Azalia controller and connects to all codecs on the link. The assertion of this signal results in all Azalia Link interface logic being reset to default “power on” state.
Azalia_SDO	Output	23	Serial Data Out: double pumped data that is sourced from Azalia compliant controller.
Azalia_SDI_A	Input/Output	26	Serial Data In 0: Point-to-point single pumped data signal. Codecs drive SDI and the Azalia controller samples SDI with respect to the rising edges of BCLK.
Azalia_SDI_B	Input/Output	24	Serial Data In 1: Point-to-point single pumped data signal. Codecs drive SDI and the Azalia controller samples SDI with respect to the rising edges of BCLK.
CD_Left	Input	13	Left audio channel from the CD ROM.
CD_Right	Input	11	Right audio channel from the CD ROM.
CD_GND	Input	9	Common mode ground connected to CD ROM ground input to provide common-mode noise rejection.

Signal Name	Type	Pin Number	Description
3.3 $V_{aux/dual}$	Supply	17	3.3 $V_{aux/dual}$ supply providing auxiliary power during system states in which ring detection is necessary. Ring detection is necessary during active states for modem operation as well as sleep states for WOR. 3.3 $V_{aux/dual}$ may optionally provide full power during system states in which the modem subsystem is active. System designers should refer to the specifics of the designs if the modem makes use of this property.
Ground	Ground	15	Power supply ground return for 3.3 $V_{aux/dual}$.
3.3 V_{main}	Supply	21	3.3 V_{main} supply providing full power during system states in which a modem or audio subsystem is active.
Ground	Ground	19	Power supply ground return for 3.3 V_{main}.
5.0 V_{main}	Supply	10	5.0 V_{main} supply provides full power during system states in which a modem or audio subsystem is active.
Ground	Ground	8	Power supply ground return for 5.0 V_{main}.
5.0 VD	Supply	18	Optional 5.0 VD supply providing full power during system states in which the audio subsystem is active. This rail will typically be sourced from the same power plane as the 5 V_{main}.
Ground	Ground	20	Power supply ground return for 5.0 VD.
Ground	Ground	3	Analog signal ground return.
Ground	Ground	28	Digital signal ground return for Azalia_BCLK.
Ground	Ground	27	Digital signal ground return for Azalia Link signals except Azalia_BCLK.
RESERVED	N/A	12	Reserved
RESERVED	N/A	14	Reserved
RESERVED	N/A	6	Reserved

3.1.3 MDC 1.5 Connector

"MDC 1.5" is a new form factor proposal for a smaller Azalia daughter card to be used in volume production systems.

The mobile daughter card 12-pin connector is the interface between the motherboard and the modem or audio circuitry located on the MDC. The connector has a low profile, 3-mm parallel board stacking height with the plug and receptacle in a tape and real packaging. The plug is shown in Figure 9 (Tyco* PN 1-179396-2) and the receptacle is shown in Figure 10 (Tyco PN 1-179397-2). These drawings are shown to represent the 12-pin solution, but scale from the higher pin-count that is shown in the drawing. Table 6 and Table 7 show the features of the connectors. Figure 11 is an example of a typical printed circuit board layout design.

Figure 9. Plug Sub Assembly Tyco PN 1-179396-2

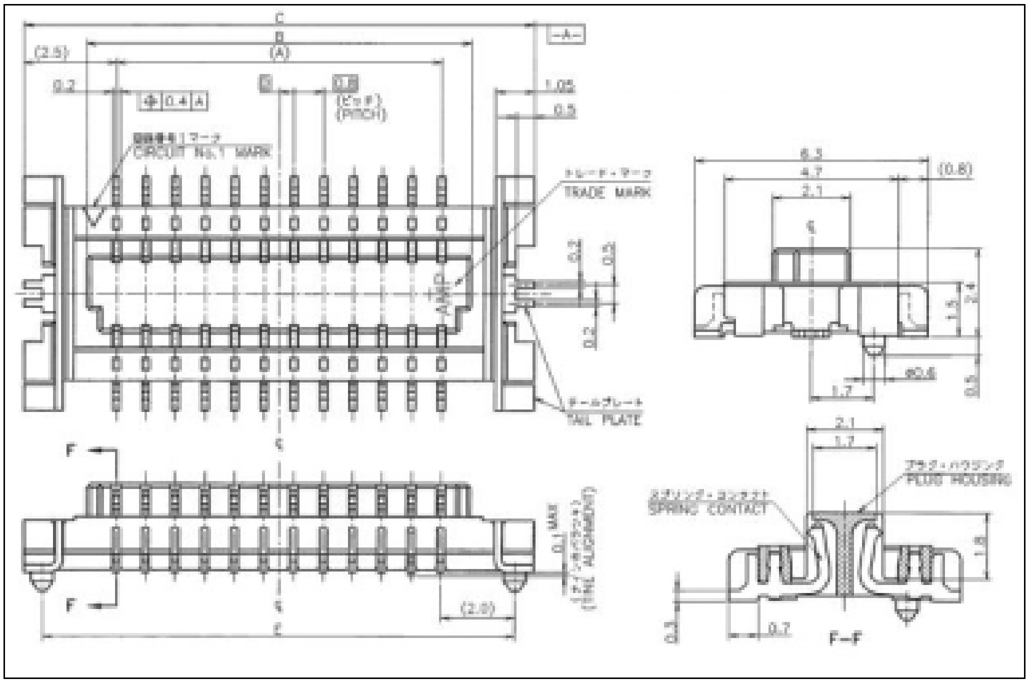


Table 6. Features of 12-Pin Tyco* SMT Connector Plug

Features Of 12-Pin AMP* Fine Pitch SMT Connector Plug	
Sex	Plug
# of Positions	12
# of Rows	Dual
Centerline Spacing	.031 [0.8] in. [mm]
Keyed	Yes
Board-to-Board Stack Height	.118 [3.00] in. [mm]
Connector Size	.031 [0.8] in. [mm]
Contact Mating Area Plating	Tin, Lead Free
Locating Posts	With
Packaging Method	Tape Mounted
Dim. A	.157 [4.00] in. [mm]
Dim. B	.218 [5.55] in. [mm]
Dim. C	.354 [9.0] in. [mm]
Dim. E	.315 [8.00] in. [mm]
Housing Material	6T Nylon
Housing Color	Natural
Housing Material Temp.	High
Contact Material	Phosphor Bronze
Solder Tail Plating	Tin, Lead Free

Figure 10. Receptacle Sub Assembly Tyco PN 1-179397-2

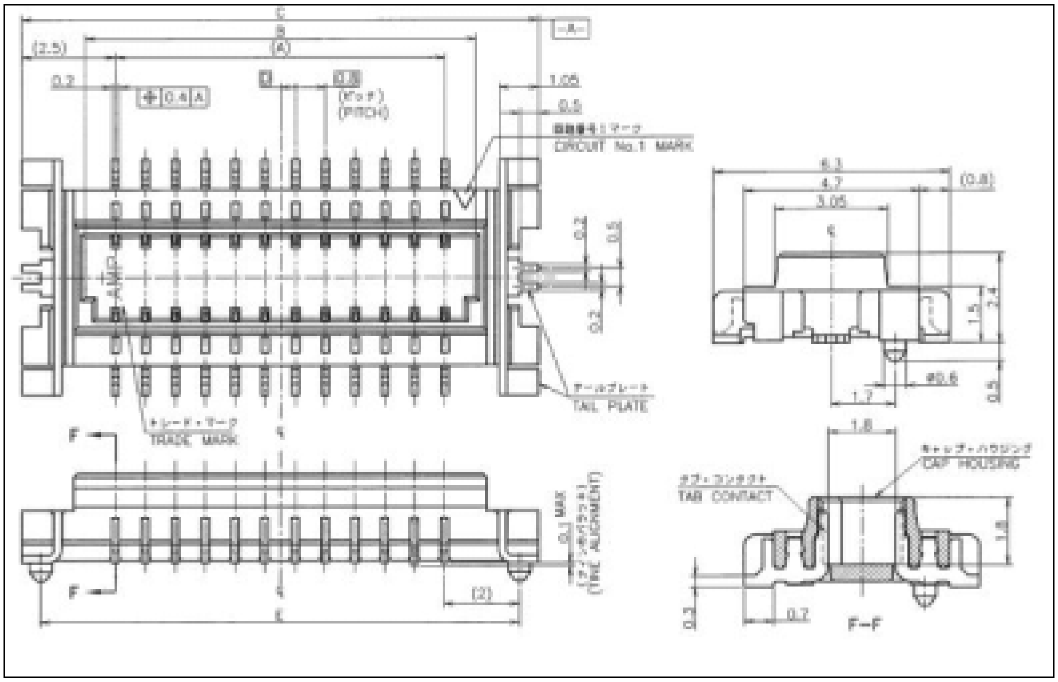
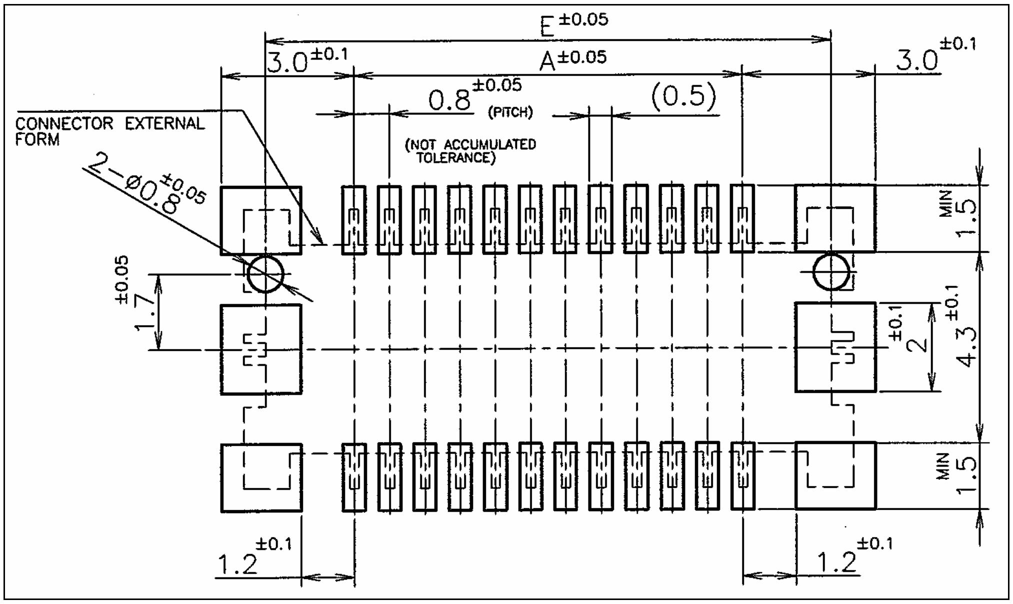


Table 7. Features of 12-Pin Tyco* SMT Connector Receptacle

Features Of 12 Pin AMP* Fine Pitch SMT Connector Receptacle	
Sex	Receptacle
# of Positions	12
# of Rows	Dual
Centerline Spacing	.031 [0.8] in. [mm]
Keyed	Yes
Board-to-Board Stack Height	.118 [3.00] in. [mm]
Connector Size	.031 [0.8] in. [mm]
Contact Mating Area Plating	Tin, Lead Free
Locating Posts	With
Packaging Method	Tape Mounted
Dim. A	.157 [4.00] in. [mm]
Dim. B	.220[5.60] in. [mm]
Dim. C	.354[9.0] in. [mm]
Dim. E	.315 [8.00] in. [mm]
Housing Material	6T Nylon
Housing Color	Natural
Housing Material Temp.	High
Contact Material	Phosphor Bronze
Solder Tail Plating	Tin, Lead Free

Figure 11. Recommended P.C. Board Footprint for the Tyco 12 pin Connector



3.1.4 MDC 1.5 Interface

The Azalia MDC 1.5 connector is smaller than the MDC 1.0 connector and is optimized for Azalia modem use. The proposed pin out for the 12-pin connector solution is shown below. Reserved pins are reserved for future changes and should not be used.

Table 8. Pin out for MDC 1.5

Pin No.	Definition	Definition	Pin No.
1	GND	RESERVED	2
3	Azalia_SDO	RESERVED	4
5	GND	3.3 Vmain/aux	6
7	Azalia_SYNC	GND	8
9	Azalia_SDI	GND	10
11	Azalia_RST#	Azalia_BCLK	12

3.1.4.1 MDC 1.5 Azalia Pin Descriptions

Table 9. Azalia Pin List for MDC 1.5

Signal Name	Type	Pin Number	Description
Azalia_BCLK	Input	12	Bit Clock: 24.00-MHz clock from the Azalia controller that connects to all codecs on the link.
Azalia_SYNC	Input	7	Signal that marks the input and output frame boundaries, as well as identifying outbound data streams. Sourced from the Azalia controller and connects to all codecs on the link.
Azalia_RST#	Input	11	Active low Azalia Link reset signal. Sourced from the Azalia controller and connects to all codecs on the link. The assertion of this signal results in all Azalia Link interface logic being reset to default "power on" state.
Azalia_SDO	Input/Output	3	Serial Data Out: double pumped data that is sourced from Azalia compliant controller.
Azalia_SDI	Input/Output	9	Serial Data In: Point-to-point single pumped data signal. Codecs drive SDI and the Azalia controller samples SDI with respect to the rising edges of BCLK.
3.3 $V_{aux/dual}$	Supply	6	3.3 $V_{aux/dual}$ supply providing auxiliary power during system states in which ring detection is necessary. Ring detection is necessary during active states for modem operation as well as sleep states for wake-on-ring. 3.3 $V_{aux/dual}$ may optionally provide full power during system states in which the modem subsystem is active. System designers should refer to the specifics of the modem design to determine if the modem makes use of this property.
Ground	Ground	8	Power supply ground return for 3.3 $V_{aux/dual}$.
3.3V_{main}	Supply	6	3.3 V_{main} supply providing full power during system states in which a modem or audio subsystem is active.
Ground	Ground	8	Power supply ground return for 3.3 V_{main}.
Ground	Ground	10	Digital signal ground return for Azalia_BCLK.
Ground	Ground	1,5	Digital signal ground return for Azalia Link signals except Azalia_BCLK.

3.1.5 Electrical Specifications

Table 10. Electrical Specifications for the MDC System Interface Connector

Signal Name	Min.	Max.	Units	Comments
Azalia_BCLK Azalia_SYNC Azalia_RST# Azalia_SDO Azalia_SDI[0..2]	-- -- -- -- --	-- -- -- -- --	-- -- -- -- --	Refer to current version of the Azalia Component Specification.

3.1.6 Power Specifications

Table 11. Power Specification for MDC

Power Rail	Min.	Max.	Units	Comments
+3.3 $V_{aux/dual}$				3.3 $V_{aux/dual}$ supply provides auxiliary power when ring detection is necessary, i.e. when the modem is active and when wake-on-ring functionality is desired. 3.3 $V_{aux/dual}$ supply may also *optionally* provide full power when the modem is active as per modem subsystem design requirements.[1]
Tolerance	--	±5	%	
Supply Current *active* auxiliary	-- --	*0.5* 3.0	*Amps* mAmps	
+3.3V_{main}				3.3 V_{main} supply providing full power when an audio or modem subsystem is active.[2]
Tolerance	--	±5	%	
Supply Current	--	0.5	Amps	
+5.0V_{main}				5 V_{main} supply providing full power when an audio or modem subsystem is active.
Tolerance	--	±5	%	
Supply Current	--	0.5	Amps	
+5.0V_D				Optional 5 V_D supply providing full power when an audio or modem subsystem is active. Available to designers choosing to implement high power amplifiers on the daughter card. Typically sourced from same power plane as 5Vmain.
Tolerance	--	±5	%	
Supply Current	--	0.5	Amps	

The audio-only MDC must have a higher supply current on the +5.0 V_{main} rail in order to meet the supply requirements of the audio subsystem. However, the maximum supply current of 500 mA may not provide enough power on the 5 V_{main} rail for an audio-only MDC that houses a high-powered stereo amplifier. As such, an additional 5 V_D supply is provided for those daughter card designs that include a high-powered stereo amplifier for internal speakers rated at greater than 1 W each.

[1] When 3.3 $V_{aux/dual}$ provides full power during the active state, the 3.3 V_{main} supply may optionally not be used and therefore be a No Connect on the motherboard and daughter card.

3.1.7 Recommended Voltages for MDC

Table 12. Recommended Voltages for MDC

Signal	+5.0 V_{main}	+3.3 V_{main}	+3.3 $V_{aux/dual}$
Azalia Link (codec signals)			
BIT_CLK		√	
SDATA_IN (audio)		√	
SDATA_IN (modem)			√
Azalia Link (controller signals)			
SYNC		√	
RESET#			√
SDATA_OUT		√	
Audio digital logic		√	
Audio analog logic	√(see text)		
Modem digital logic		√	
Modem analog circuitry	√(see text)		
Modem wake logic			√

The +5.0 V_{main} and the +3.3 V_{main} rails as well as the optional +5 V_D rail are available to power the analog portion of the audio codec and peripheral audio circuitry. It is the responsibility of the daughter card manufacturer to provide a "clean" power supply derived from the digital supply to the analog circuitry. The quality of the audio subsystem is in part dependent upon the purity of the derived analog power supply.

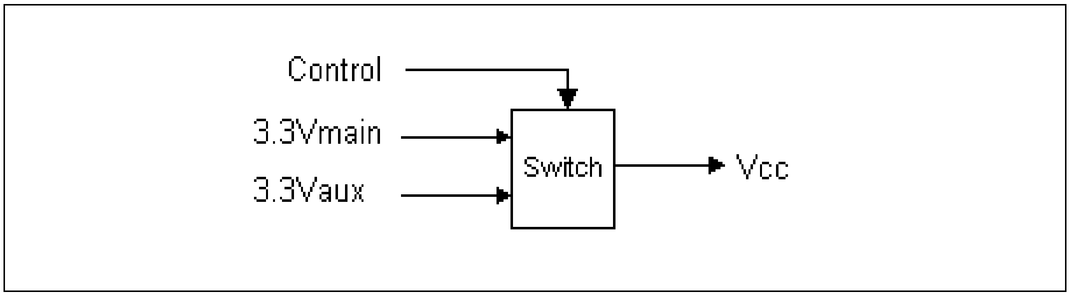
Figure 12 below depicts the power distribution to enable audio and modem functionality, including wake-on-ring, on the MDC.

Both the +5.0 V_{main} and +3.3 V_{main} rails are available to power the analog portion of the modem subsystem that is not necessary for wake-on-ring. No part of the modem subsystem necessary for wake-on-ring functionality should draw from the +5.0 V_{main} or +3.3 V_{main} power supply, including the ring detection circuitry of the DAA, since these rails are shut down in low power system states.

All audio driven Azalia Link signals, as well as other digital logic associated with the audio subsystem, must be powered by a +3.3V rail. Both the +5.0 V_{main} and +3.3 V_{main} as well as the 5 V_D rail are available to power the analog portion of the audio codec and peripheral audio circuitry.

The 3.3 $V_{aux/dual}$ rail can either be supplied by the 3.3 V auxiliary rail ***or*** a combination of the 3.3 V_{main} and 3.3 V_{aux} rails as shown below in Figure 12. The switch can be any implementation that results in a muxing of the main and auxiliary power supplies. This switch can be controlled via a power management signal or GPIO.

Figure 12. Switching Algorithm for 3.3-V Dual Operation



Since the logic necessary for a ring detection is also necessary during active operation of the modem, the +3.3 $V_{aux/dual}$ supply must ***at minimum*** provide the auxiliary current during all system states and may ***optionally*** provide full power as per the modem subsystem design requirements specified by the modem vendor/manufacturer.

The system designer is responsible for coordinating with the modem vendor/manufacturer to provide the necessary current via the +3.3 $V_{aux/dual}$ rail when wake-on-ring is desired as modem implementations may require less than the 3.0-mA maximum.

4 Mechanical Requirements

4.1 MDC Layout

Depending on the design, there are two specific form factors. The MDC 1.0 can apply to audio, modem, or audio and modem codec solutions, and the MDC 1.5 applies to modem or audio codec solutions.

If designing a modem the form factor should be chosen carefully. Having the added flexibility of two form factors also adds risk that there could be an Azalia MDC design that meets the specification, but will not work in a given design due to a connector mismatch. For example, where space is premium, Azalia MDC 1.5 designs are expected to only appear in thin and light notebook designs.

All dimension labels are in millimeters with a tolerance of ±0.25 mm.

4.1.1 Telephone and Audio Jacks

The MDC with jacks module option allows the housing of one RJ11 jack with surge protection circuitry and up to three audio mini-jacks. The RJ11 jack is from Hirose* (Part Number TM18R-62) or equivalent. The audio mini-jack is from Foxconn* (Part Number JA6033L) or equivalent.

4.1.2 MDC 1.0 Dimensions

Figure 13 (with jacks option) and Figure 14 (without jacks option), show the placement of the system connectors and drill holes on the MDC. The system connector is mounted on the ***bottom*** of the daughter card in order to minimize the height of the module. The overall dimensions of the MDC module is 73.5 mm width x 55 mm length x 5.0 mm height. Figure 14 (with jacks option) shows another drill hole placed in the left hand corner of the MDC in order to provide further support for the jacks.

Figure 13. Mechanical Dimensions for MDC with Jacks (Top View)

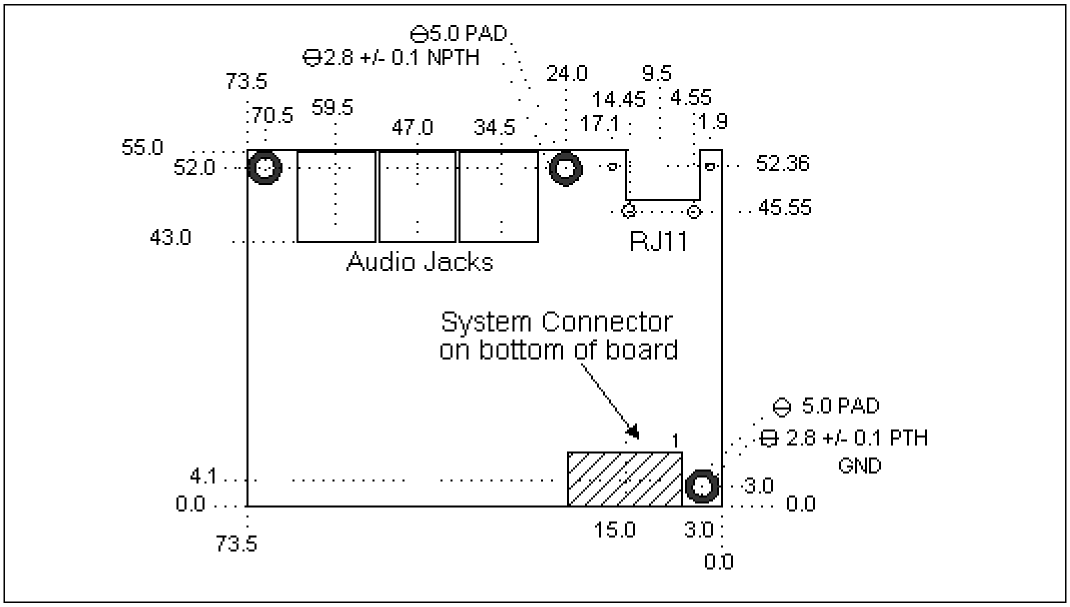


Figure 14. Mechanical Dimensions for MDC without Jacks (Top View)

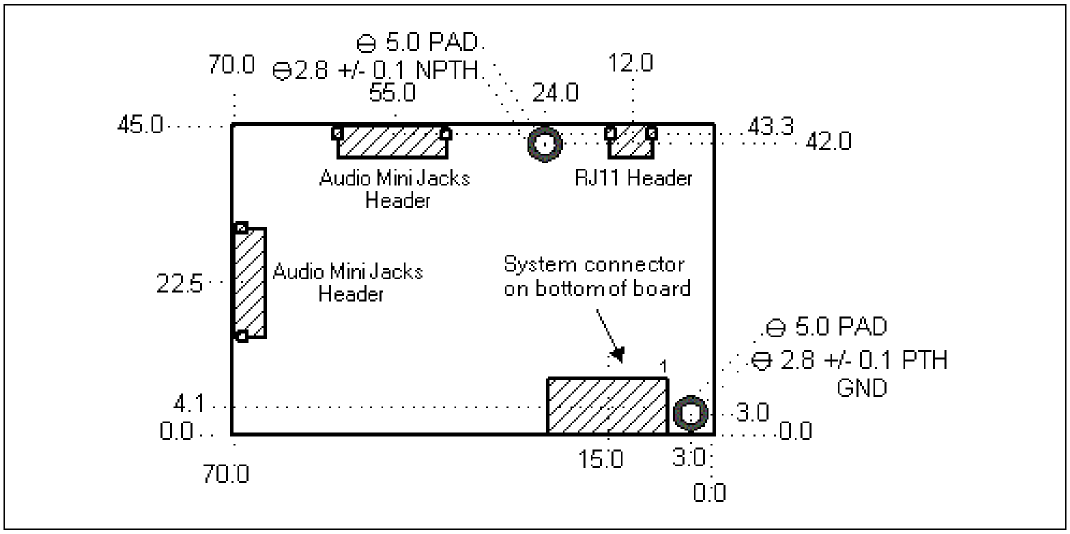
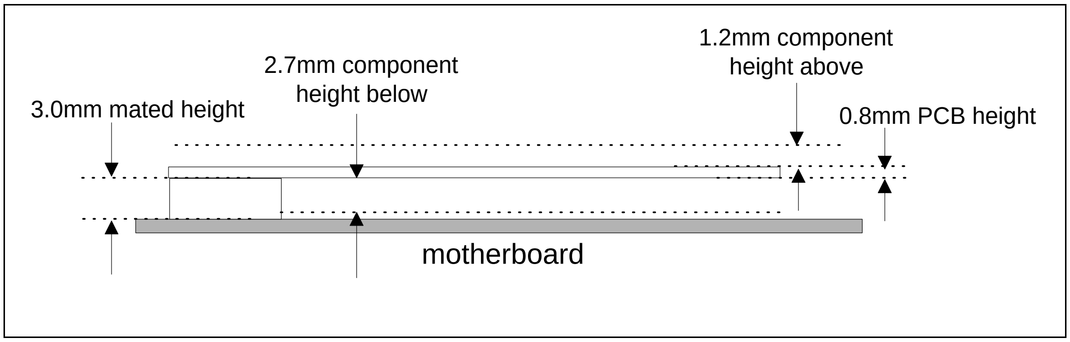


Figure 15 details the component height restrictions of the MDC. The mated height of the system interface connector is variable and is shown here at its minimum of 3.0 mm. The through hole adjacent to the 30-pin system connector is plated for connection to ground.

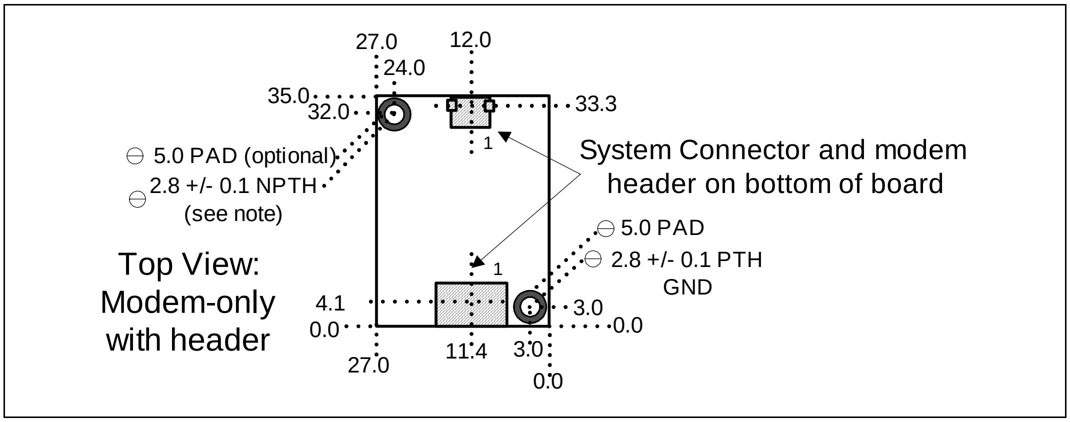
Figure 15. Component Height Restrictions for MDC with Header (Side View)



4.2 MDC 1.5 Dimensions

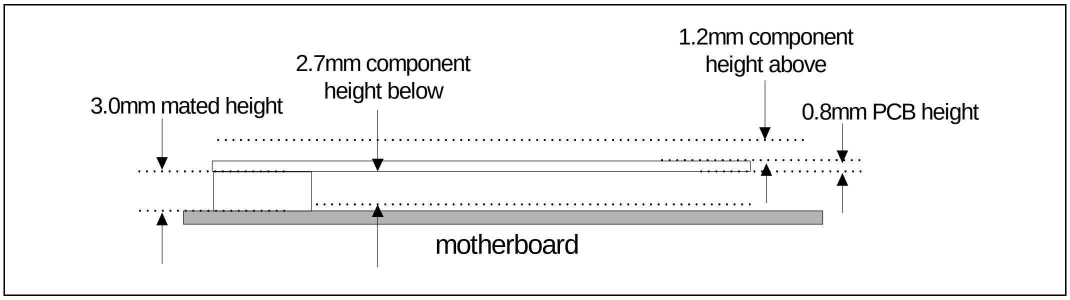
The following figure shows the placement of the system connectors and drill holes on the MDC 1.5. The system connector is mounted on the ***bottom*** of the daughter card in order to minimize the height of the module. The overall dimensions of the MDC 1.5 module is 27.0 mm width x 35.0 mm length x 5.0 mm height.

Figure 16. Mechanical Dimensions for MDC 1.5 (Top View)



The following figure details the component height restrictions of the MDC. The mated height of the system interface connector is variable and is shown here at its minimum of 3.0 mm. The through hole adjacent to the 20-pin system connector is plated for connection to ground.

Figure 17. Component Height Restrictions for MDC 1.5 with Header (Side View)



4.3 MDC Header Configuration

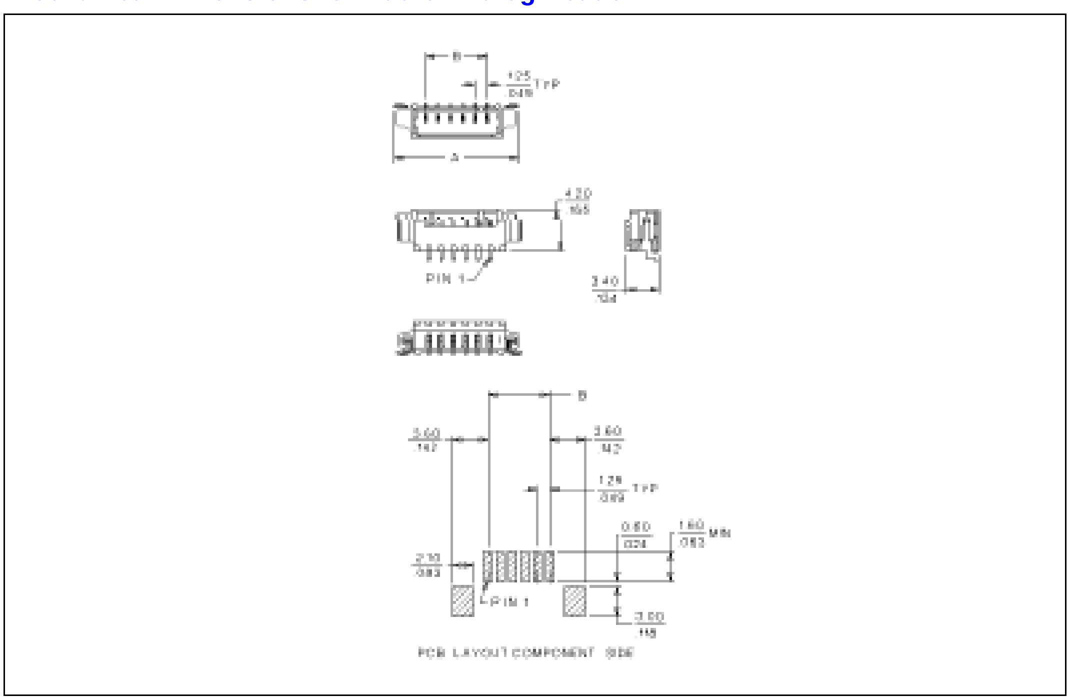
4.3.1 Audio Analog Header

If audio mini jacks are not incorporated in the MDC design, the appropriate signals can be routed to two, 12-pin headers on the daughter card. This header will be used to cable the signals to audio mini jacks on the Mott Canyon 2 test card. The headers are 12-pin.53261-1290 Molex* parts.

Table 13. Pin Out for Headers to Audio Mini Jacks

AUDIO HEADER 1		AUDIO HEADER 2	
Pin Number	**Signal**	**Pin Number**	**Signal**
1	Stereo Jack B Left	1	Stereo Jack F Left
2	Stereo Jack B Right	2	Stereo Jack F Right
3	Ground	3	Ground
4	Stereo Jack C Left	4	Stereo Jack G Left
5	Stereo Jack C Right	5	Stereo Jack G Right
6	Ground	6	Ground
7	Stereo Jack D Left	7	Stereo Jack H Left
8	Stereo Jack D Right	8	Stereo Jack H Right
9	Ground	9	Ground
10	Stereo Jack A Left	10	Stereo Jack E Left
11	Stereo Jack A Right	11	Stereo Jack E Right
12	Jack Sense A-D	12	Jack Sense E-H

Figure 18. Mechanical Dimensions for Audio Analog Header



4.3.2 Modem Analog Header

If an RJ11 jack is not incorporated in the design of the MDC, the appropriate signals can be routed to a header on the daughter card. The header for the phone jack is a 2 pin JAE* header (part number FI-S02P-HF) with the following pin-out. The JAE* FI series accepts 28 to 32 gauge wire for cabling.

Table 14. Pin Out for Header to RJ11 Jack

Pin Number	Signal
1	Tip
2	Ring

4.3.3 S/PDIF Header

If S/PDIF jacks are required in the design of the MDC, the appropriate signals can be routed to a 6 pin header on the daughter card. This header will be used to cable the signals to the S/PDIF jacks on the riser test card.

Table 15. Pin Out for Header to S/PDIF Jacks

Pin Number	Signal
1	S/PDIF Out
2	No Connect
3	Ground
4	Head Phone Detect
5	Line Out Detect
6	S/PDIF In

4.4 EFI, RFI, Shielding Requirements

It is the responsibility of the mobile daughter card designer to ensure that the daughter card does not prevent a system from meeting the required regulatory requirements concerning EMI and RFI.

5 BIOS/Software Requirements

A mobile daughter card based audio and/or modem subsystem must always be configured as a motherboard integrated subsystem. The mobile daughter card vendor is responsible for development of all drivers and/or BIOS code needed to configure and manage the mobile daughter card based subsystem hardware resources.